IEEE Journal of Emerging and Selected Topics in Industrial Electronics

Special Section on

Advanced Hardware-in-the-Loop Methodologies for Breakthrough Validation and Testing of Next Generation Power Systems

(Sponsored by IEEE IES TC on Smart Grids)

Power system validation approaches such as digital real-time simulation (DRTS), controller hardware-in-the-loop (CHIL), power hardware-in-the-loop (PHIL), and geographically distributed real-time simulation (GDRTS) have played a vital role in supporting development and deployment of novel technologies in the power industry, attracting significant interest from academic researchers and industrial practitioners alike. However, the complexity of power systems is rapidly increasing with the fast emergence of a smarter grid accommodating ever-high penetrations of distributed generation, novel control and protection devices, and advanced monitoring systems in the run-up to realizing net-zero targets. This increasing complexity presents novel challenges to existing power system validation approaches.

To support the smooth transition to net-zero power systems at pace, there is a growing need for novel techniques of DRTS and hardware-in-the-loop (HIL) methodologies. Techniques and methods that allow for the identification of the intricate dependencies and interactions of the holistic power systems and enable the testing of the interactions between the physical power apparatus/network and the complex systems over broad operating conditions are required. Hence, this special section aims to present novel contributions, new methodologies, and advanced setups that address key challenges of real-time hardware-in-the-loop approaches for the validation of complex power systems and future smarter grids. Issues such as stability, accuracy, and practical implementation of new interface algorithms, as well as the application of HIL simulation to emerging research problems in the field of power systems, are particularly expected to be accommodated throughout this special section, while extended HIL setups (e.g., with multiple power amplifiers or extended hardware under test) will be of special interest for the guest editorial committee as well.

We encourage all researchers working in this area to submit papers to this Special Section. Topics of interest include, but are not limited to:

- ✓ **Novel real-time simulation concepts and applications**
- ✓ **Interface algorithms for distributed real-time simulation**
- ✓ **Novel CHIL methodologies and applications**
- ✓ **Advanced interface algorithms for PHIL**
- ✓ **Stability, accuracy, and sensitivity considerations in DRTS/CHIL/PHIL/GDRTS setups**
- ✓ **Testing of novel inverter control schemes (e.g., grid-forming or black-start) through PHIL setups**
- ✓ **Testing of novel smart grid protection schemes through CHIL setups**
- ✓ **Prototype power amplifiers for low-cost PHIL simulation implementation**
- ✓ **DRTS/CHIL and PHIL methods in the engineering education sector**

Manuscript Preparation and Submission

Check carefully the style of the journal described in the guidelines “Information for Authors” on the IEEE- IES website http://www.ieee-ies.org/pubs/jestie. Please submit your manuscript in electronic form through https://mc.manuscriptcentral.com/jestie-ieee.

On the submitting page, in the pop-up menu of the manuscript type, select: “**SS on Advanced Hardware-in-the-Loop Methodologies for Breakthrough Validation and Testing of Next Generation Power Systems**”, then upload all your manuscript files following the instructions.

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Timetable

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